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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/494,567	01/31/2000	Martin Vorbach	2885/29	3627

26646 7590 03/08/2005

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EXAMINER	
MEONSKE, TONIA L	
ART UNIT	**PAPER NUMBER**
2183	

DATE MAILED: 03/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/494,567	VORBACH ET AL.	
	Examiner	Art Unit	
	Tonia L Meonske	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 February 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *12-15,17-19 and 21-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *12-15,17-19 and 21-37* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 12-15,17-19 and 21-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Casselman, US Patent 5,802,290, in view of Rodgers et al., US Patent 5,889,982, Schrofer, US Patent 4,682,284, and Cooke et al., US Patent 5,970,254.

3. Referring to claim 25, Cassleman has taught a system for run-time reconfiguration of a programmable unit, the programmable unit including a plurality of reconfigurable function cells in a multidimensional arrangement (Casselman, abstract, Figure 3), comprising:

a. a primary logic unit in communication with at least one of the plurality of reconfigurable function cells, the primary logic unit configured to detect an event and to detect a state of the at least one of the plurality of reconfigurable function cells (Casselman, Figure 5, column 3, lines 14-21, column 4, lines 35-46);

b. a first memory configured to store a first configuration data associated with a selected one of the plurality of reconfigurable function cells (Casselman, Figure 4, The memory area where the configuration bit files that are produced by the mother FPGA are stored.); and

c. the primary logic unit configured to reconfigure the selected one of the plurality of reconfigurable function cells if the selected one of the plurality of reconfigurable

function cells is in a reconfigurable state (Casselman, Figure 5, column 3, lines 14-21, column 4, lines 35-46).

4. Casselman has not specifically taught a jump table coupled to the primary logic unit having a plurality of entries, at least one of the plurality of entries configured to store a memory address of the first configuration data, wherein when the primary logic unit detects the event, the primary logic unit calculates the address of the at least one of the plurality of entries in the jump table based on a source of the event, retrieves the memory address, and retrieves the stored first configuration data based on the memory address. Casselman has taught that rapidly transitioning between operating modes, or configuration modes, is desirable (Column 3, lines 4-20).

5. Rodgers has taught an efficient method for transitioning between operating modes. Rodgers has taught a jump table coupled to the primary logic unit having a plurality of entries(Rodgers et al., column 16, line 50-column 17, line 3), at least one of the plurality of entries configured to store a memory address of the first configuration data (Rodgers et al., column 16, line 50-column 17, line 3), wherein when the primary logic unit detects the event, the primary logic unit calculates the address of the at least one of the plurality of entries in the jump table based on a source of the event (Rodgers et al., column 16, line 50-column 17, line 3, The exception vector is the address for the entry in the event ROM. The address is calculated based on the source of an event, or type of exception.), retrieves the memory address, and retrieves the stored first configuration data based on the memory address (Rodgers et al., Abstract, column 16, line 50-column 17, line 3, In order to invoke the microcode event handler the entry in the table must be retrieved.) in order to service mode switching events efficiently (Rodgers et al., column 17, lines 29-41). It would have been obvious to one of ordinary skill in the art at the time the

invention was made to incorporate the efficient method of transitioning between operating modes using look-up tables, as taught by Rodgers et al., into the invention of Casselman, for the desirable purpose of rapidly transitioning between varying configuration modes of the PLU's.

6. Furthermore, Casselman has not taught a FIFO memory coupled to the primary logic unit configured to store a plurality of configuration data associated with the plurality of reconfigurable function cells, the plurality of configuration data including the first configuration data, the first configuration data stored in the FIFO memory if the selected one of the plurality of reconfigurable function cells is not in a reconfiguration state, and the primary logic unit configured to reconfigure the selected one of the plurality of reconfigurable function cells if the selected one of the plurality of reconfigurable function cells is in a reconfigurable state. However, Shrofer has taught a FIFO memory coupled to the primary logic unit configured to store a plurality of data associated with a plurality of function cells including a first data (Schrofer, Abstract Figure 3, element 301, Column 2, lines 29-34). Shrofer has further taught the first data is stored in the FIFO memory if the selected one of the plurality of function cells is busy (Schrofer, Abstract Figure 3, element 301, Column 2, lines 29-34, column 5, lines 40-50, If the executing apparatus is not ready to receive requests, then the request is stored in the queue for later processing.) for the desirable purpose of being able to queue up requests to the executing apparatus even when the executing apparatus is not ready itself to accept requests (Column 5, lines 40-50). . It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the invention of Casselman, include the claimed one or more FIFO memory areas, as taught by Shrofer, for the desirable purpose of being able to queue up configuration data to the PLU's even when the PLU's cannot currently be reconfigured

(Column 5, lines 40-50) so that the system may continue processing data even when the PLU's are not ready to be reconfigured.

7. Furthermore, Casselman has not taught that the memory that stores configuration data is shard by a plurality of reconfigurable function cells. However, Cooke et al. have taught a memory that stores configuration data is shared by a plurality of reconfigurable cells (Cook et al., abstract) for the desirable purpose of allowing efficient use of the memory. Therefore it would have been obvious to one of ordinary skilli in the art at the time the invention is made to have the memory that store configuration data of Casselman, be shared by a plurality of reconfigurable cells, as taught by Cook et al. (Cook et al., abstract) for the desirable purpose of allowing efficient use of the memory.

8. Referring to claim 26, Casselman has taught the system according to claim 25, as described above, and wherein the first memory is configured to store a plurality of configuration data, at least one configuration data from the plurality of configuration data including a complete configuration of the at least one of the plurality of reconfiguration function cells (Column 12, lines 18-39, When an FPGA is reconfigured to implement a user selected algorithm, the configuration memory stores a complete configuration bit file.).

9. Referring to claim 27, Casselman in combination with Rodgers et al. and Shrofer have taught the system according to claim 25, as described above, and wherein the first memory is configured to store at least one subconfiguration data configured to represent only a part of a complete configuration of the at least one of the plurality of reconfiguration function cells (Column 12, lines 18-39, When an FPGA is reconfigured to implement only a portion of a user

selected algorithm, the configuration memory stores a subconfiguration representing only a part of a complete configuration of the units.).

10. Referring to claim 28, Casselman in combination with Rodgers et al. and Shrofer have taught the system according to claim 25, as described above, and wherein the primary logic unit contains a start configuration register which points to a start configuration that puts the at least one of the plurality of reconfiguration function cells in a valid state (Rodgers et al., column 16, line 50-column 17, line 3, The entry read out of the table points at a start configuration that puts the units in a valid state.).

11. Referring to claim 29, Casselman in combination with Rodgers et al. and Shrofer have taught the system according to claim 25, as described above, and wherein the primary logic unit contains a FIFO start register which points to a start of a memory area to which a configuration data is copied (Schrofer, Column 9, lines 5-30).

12. Referring to claim 30, Casselman in combination with Rodgers et al. and Shrofer have taught the system according to claim 25, as described above, and wherein the primary logic unit contains a FIFO end register which points to an end of a memory area to which a configuration data is copied (Schrofer, Column 9, lines 30-57, Column 12, lines 57-63).

13. Referring to claim 31, Casselman in combination with Rodgers et al. and Shrofer have taught the system according to claim 25, as described above, and wherein the primary logic unit contains a FIFO free entry register which points to a free entry of a memory area to which a configuration data is copied and which is closest to a start of the memory area (Schrofer, Column 9, lines 30-57).

14. Referring to claim 32, Casselman in combination with Rodgers et al. and Shrofer have taught the system according to claim 25, as described above, and wherein the primary logic unit contains a program counter register which points to an entry to be processed within the first memory (Rodgers et al., Abstract, column 16, line 50-column 17, line 3, The register which holds the pointer to the jump table.)

15. Referring to claim 33, Casselman in combination with Rodgers et al. and Shrofer have taught the system according to claim 25, as described above, and wherein the primary logic unit contains an address register which points to an address of the cell which has triggered the event (Rodgers et al., Abstract, column 16, line 50-column 17, line 3, The address of the cell which triggered an event must inherently be stored in a register.).

16. Referring to claim 34, Casselman in combination with Rodgers et al. and Shrofer have taught the system according to claim 25, as described above, and wherein the primary logic unit contains a data register containing a configuration data which is transmitted to the at least one of the plurality of reconfiguration function cells in a reconfiguration (Casselman, Figure 4, The register where the configuration bit files that are produced by the mother FPGA are stored.).

17. Referring to claim 35, Casselman in combination with Rodgers et al. and Shrofer have taught the system according to claim 25, as described above, and wherein the primary logic unit contains a dispatch register which contains the address of an entry in the jump table calculated from a cell address (Rodgers et al., Abstract, column 16, line 50-column 17, line 3, The address of the entry must inherently be stored in a register.).

18. Claim 12 does not recite limitations above the claimed invention set forth in claim 25 and is therefore rejected for the same reasons set forth in the rejection of claim 25 above.

19. Referring to claim 13, Casselman in combination with Rodgers et al. and Shrofer have taught the system according to claim 12, as described above, wherein, when the primary logic unit detects the event (When the PLU of Casselman needs reconfigured. Also see Shrofer, column 3, lines 48-57), the primary logic unit reads the FIFO memory to determine whether a configuration data from the plurality of configuration data is stored in the FIFO memory (Schrofer, Abstract, Columns 2 and 3, Column 2, lines 29-34).

20. Referring to claim 14, Casselman in combination with Rodgers et al. and Shrofer have taught the system according to claim 13, as described above, and wherein, when the primary logic unit determines that no configuration data is stored in the FIFO memory (Schrofer, Abstract, Columns 2 and 3, Column 2, lines 29-34), the primary logic unit retrieves the memory address (Casselman, Figure 4, The address of the memory area where the configuration bit files that are produced by the mother FPGA is retrieved.), retrieves the first configuration data from the first memory based on the memory address (Casselman, Figure 4, In order to reconfigure the FPGA the configuration bit file must inherently be retrieved.), and one of reconfigures the selected one of the plurality of reconfigurable function cells based on the configuration data if the selected one of the plurality of reconfigurable function cells is in a reconfigurable state (Figure 4), and stores the first reconfiguration data in the FIFO memory if the selected one of the plurality of reconfigurable function cells is not in a reconfigurable state (Schrofer, Abstract, Columns 2 and 3, Column 2, lines 29-34).

21. Referring to claim 15, Casselman in combination with Rodgers et al. and Shrofer have taught the system according to claim 13, as described above, and wherein, when the primary logic unit determines that some configuration data from the plurality of configuration data is

stored in the FIFO memory, if the first configuration data is not stored in the FIFO memory, the primary logic unit retrieves the first configuration data from the first memory based on the memory address, and stores the first configuration data in the FIFO memory (Schrofer, Abstract, Columns 2 and 3, Column 2, lines 29-34, The FIFO is queued up with configuration data.).

22. Referring to claim 17, Casselman in combination with Rodgers et al. and Shrofer have taught the system according to claim 13, as described above, and wherein, when the primary logic unit determines that some configuration data from the plurality of configuration data is stored in the FIFO memory, if the first configuration data is stored in the FIFO memory and is not the first entered into the FIFO memory, the primary logic unit does not retrieve the first configuration data (Schrofer, Abstract, Columns 2 and 3, Column 2, lines 29-34, This claim is merely the definition of a FIFO.).

23. Claim 18 does not recite limitations above the claimed invention set forth in claim 25 and is therefore rejected for the same reasons set forth in the rejection of claim 25 above.

24. Claim 19 does not recite limitations above the claimed invention set forth in claim 13 and is therefore rejected for the same reasons set forth in the rejection of claim 13 above.

25. Claim 21 does not recite limitations above the claimed invention set forth in claim 14 and is therefore rejected for the same reasons set forth in the rejection of claim 14 above.

26. Claim 22 does not recite limitations above the claimed invention set forth in claim 15 and is therefore rejected for the same reasons set forth in the rejection of claim 15 above.

27. Claim 23 does not recite limitations above the claimed invention set forth in claim 16 and is therefore rejected for the same reasons set forth in the rejection of claim 16 above.

28. Claim 24 does not recite limitations above the claimed invention set forth in claim 17 and is therefore rejected for the same reasons set forth in the rejection of claim 17 above.

29. Claim 36 does not recite limitations above the claimed invention set forth in claims 14 and 25 is therefore rejected for the same reasons as set forth in claims 14 and 25.

30. Claim 37 does not recite limitations above the claimed invention set forth in claims 25, 12, 13, and 14 is therefore rejected for the same reasons as set forth in claims 25, 12, 13, and 14.

Response to Arguments

31. Applicant's arguments with respect to claims 12-15,17-19 and 21-37 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

32. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tonia L Meonske whose telephone number is (571) 272-4170. The examiner can normally be reached on Monday-Friday, 8-4:30.

33. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie P Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

34. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

tlm

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